



SPECIALTY Products CMOS EEPROM Selection Guide

General Description

National Semiconductor offers a full line of CMOS EEPROMs. Some share the MICROWIRE™ Serial Interface such as the NM83C208 and the NM83C206; others share the I²C (2-wire) interface such as the NM24C02 and the NM24C08. In addition to the above EEPROMs, we also offer some specialty EEPROMs.

These include the NM85C12, NM83C46A and the NM25C04 EEPROMs.

The NM85C12 is a 976-bit CMOS EEPROM with 8 programmable outputs that can be used as switches, i.e., DIP or analog. The 976 bits of memory are divided into 81 registers of 16 bits each with each register individually accessible. Registers 81-83 are dedicated for DIP switch functions. The NM85C12 contains 8 individually programmable outputs which can be used as switches.

The NM25C04 is 4096 bits of CMOS EEPROM with an SPI interface. The device is designed to seamlessly interface with the 88HCXX family of Motorola microcontrollers.

Available Product

Packages	Temperature Ranges	4.5V-5.5V	2.5V-5.5V
NM85C12	N, M	Y	Y
NM83C46A	N, M8	Y	Y
NM25C04	N, M		Y

Features

- No erase necessary
- MICROWIRE compatible interface
- Self-limited programming cycle
- 40 years data retention
- Endurance: 10⁶ data changes
- Reliable CMOS floating gate technology

The NM83C46A is 1024 bits of CMOS EEPROM which can be organized as either 64 16-bit registers or as 128 8-bit registers. The NM83C46A shares the MICROWIRE interface and the x8 and x16 configuration. The differentiating feature is in the pin configuration: The NM83C46A's Program/Erase status is output on the Data-Out (DO) pin. The device uses a low to high transition on the clock (SK) to clock all data into or out of the device, except device programming status which is independent of the clock.



NM93C06/C46/C56/C66 256-/1024-/2048-/4096-Bit Serial EEPROM (MICROWIRE™ Bus Interface)

General Description

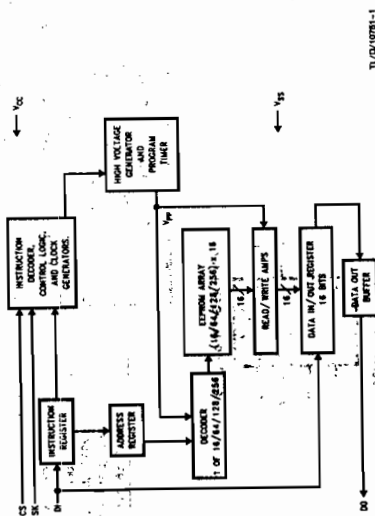
The NM93C06/C46/C56/C66 devices are 256/1024-/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. These memory devices are available in an SO package for small space considerations.

The EEPROM interfacing is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Write All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin during programming.

Features

- Device status during programming mode
- Typical active current of 400 μ A; Typical standby current of 25 μ A
- No erase required before write
- Reliable CMOS floating gate technology
- 4.5V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-limited programming cycle
- 40 years data retention
- Endurance: 10⁶ data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (Ms)



Top View

See NS Package Number N08E and M08A

TU/D/0931-2

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number*
NM93C06N/NM93C46N
NM93C06B/NM93C46B
NM93C06M/NM93C46M
NM93C56M/NM93C66M

Extended Temp. Range (-40°C to +85°C)

Order Number*
NM93C06EN/NM93C46EN
NM93C06BN/NM93C46BN
NM93C06EM/NM93C46EM
NM93C56EM/NM93C66EM

*For 14-Pin SO, availability contact your local National Semiconductor Sales Office.

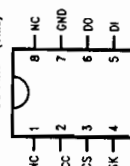
Alternate (Turned) 90 Pinout

Order Number
NM93C06TM8/NM93C46TM8/NM93C56TM8
NM93C06EM8/NM93C46EM8/NM93C56EM8

Military Temp. Range (-55°C to +125°C)

Order Number*
NM93C06MN/NM93C46MN
NM93C56MN/NM93C66MN
NM93C06MM/NM93C46MM
NM93C56MM/NM93C66MM

Alternate SO Pinout (TM8)



See NS Package M08A

TU/D/0931-12

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature
-65°C to +150°C
+6.5V to -0.3V

All Input or Output Voltages
with Respect to Ground

ESD Rating
Lead Temp. (Soldering, 10 sec.)
+300°C
200W

Operating Conditions

Ambient Operating Temperature
NM93C06-NM93C66
-40°C to +85°C

NM93C06M-NM93C66M
-55°C to +125°C

Power Supply (V_{CC})
4.5V to 5.5V

DC and AC Electrical Characteristics

V_{CC} = 5.0V ± 10% unless otherwise specified

Note: Throughout this table, "f_{sk}" refers to temperature range (-55°C to +125°C), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I _{CCA}	Operating Current	NM93C06-NM93C06B NM93C06E-NM93C06E NM93C06M-NM93C06M	CS = V _{ih} , SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		1 1	mA
I _{CCS}	Standby Current	NM93C06-NM93C06B NM93C06E-NM93C06E NM93C06M-NM93C06M	CS = V _{il}		50 50 100	µA
I _{ih}	Input Leakage		V _{ih} = 0V to V _{CC} (Note 4)		±1	µA
I _{ol}	Output Leakage			-0.1 2	0.8 V _{CC} + 1	V
V _{ih}	Input High Voltage					V
V _{oh1}	Output Low Voltage		I _{OL} = 2.1 mA		0.4	V
V _{oh1}	Output High Voltage		I _{OH} = -400 µA	2.4		V
V _{oh2}	Output Low Voltage		I _{OL} = 10 µA		0.2	V
V _{oh2}	Output High Voltage		I _{OH} = -10 µA	V _{CC} - 0.2		V
f _{sk}	SK Clock Frequency	NM93C06-NM93C06B NM93C06E-NM93C06E NM93C06M-NM93C06M	(Note 5)	0 0	.1 1 0.5	MHz
t _{skH}	SK High Time	NM93C06-NM93C06B NM93C06E-NM93C06E NM93C06M-NM93C06M		250 300 500		ns
t _{skL}	SK Low Time			250		ns
t _{skS}	SK Setup Time		SK must be at V _{ih} for t _{skS} before CS goes high	50		ns
t _{CS}	Minimum CS Low Time	NM93C06-NM93C06B NM93C06E-NM93C06E NM93C06M-NM93C06M	(Note 2)	250 250 500		ns

Functional Description

The NM93C06/C46/C56 devices have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the C06 and C46 the next 8 bits carry the op code and the 6-bit address for register selection. For the C56 and C66 the next 10-bits carry the op code and the 8-bit address for register selection.

All data in signals are clocked into the device on the low-to-high SK transition.

Read (READ):

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (WEN):

When Vcc is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (WEN) instruction. This instruction enables the internal data programming memory remains enabled until an Erase/Write Disable (WDS) instruction is executed or Vcc is completely removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the selected register to the logical "1" state. CS is brought low following the loading of the first address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the tCS interval. DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that programming is complete.

NOTE: The ISC CMOS EEPROMs do not require an "ERASE" or "ERASE ALL" operation prior to the "WRITE" and "WRITE ALL" instructions. The ERASE and "ERASE ALL" instructions are included to maintain compatibility with earlier technology EEPROMs.

Instruction Set for the NM93C06 and NM93C46

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5-A0		Reads data stored in memory, at specified address.
WEN	1	00	11XXXX		Enable all programming modes.
ERASE	1	11	A5-A0		Erase selected register.
WRITE	1	01	A5-A0	D15-D0	Writes selected register.
ERALL	1	00	10XXXX		Erases all registers.
WDS	1	00	00XXXX	D15-D0	Writes all registers.
	1	00	00XXXX		Disables all programming modes.

Note: Address bits A5 and A4 become "Don't Care" for the NM93C06.

Instruction Set for the NM93C56 and NM93C66

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7-A0		Reads data stored in memory, at specified address.
WEN	1	00	11XXXXXX		Enable all programming modes.
ERASE	1	11	A7-A0		Erase selected register.
ERALL	1	00	10XXXXXX		Erases all registers.
WRITE	1	01	A7-A0	D15-D0	Writes all registers.
WRALL	1	00	01XXXXXX	D15-D0	Writes all registers.
WDS	1	00	00XXXXXX		Disables all programming modes.

Note: Address bit A7 becomes "Don't Care" for the NM93C56.

DC and AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$ (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t _{CS}	CS Setup Time	NM93C06-NM93C06 NM93C06E-NM93C06E NM93C06M-NM93C06M		50		ns
t _{OH}	DO Hold Time			70		ns
t _{CS}	DI Setup Time	NM93C06-NM93C06 NM93C06E-NM93C06E NM93C06M-NM93C06M		100		ns
t _{CSH}	CS Hold Time			200		ns
t _{OH}	DI Hold Time			0		ns
t _{PD1}	Output Delay to "1"	NM93C06-NM93C06 NM93C06E-NM93C06E NM93C06M-NM93C06M		20		ns
t _{PD0}	Output Delay to "0"				500	ns
		NM93C06-NM93C06 NM93C06E-NM93C06E NM93C06M-NM93C06M			500	ns
t _{SV}	CS to Status Valid				1000	ns
		NM93C06-NM93C06 NM93C06E-NM93C06E NM93C06M-NM93C06M			500	ns
t _{DF}	CS to DO in Tri-State*		CS = V _L		100	ns
		NM93C06-NM93C06 NM93C06E-NM93C06E NM93C06M-NM93C06M			100	ns
t _{WC}	Write Cycle Time				200	ns
		NM93C06-NM93C06 NM93C06E-NM93C06E NM93C06M-NM93C06M			10	ns

Capacitance (Note 3)

T_A = 25°C f = 1 MHz

Symbol	Test	Typ	Max	Units
C _{OUT}	Output Capacitance		5	pF
C _{IN}	Input Capacitance		5	pF

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Note 2: CS (chip select) should be brought low (to V_L) for an interval of t_{CS} prior to an interval of t_{CSH} to ensure proper operation of the device.

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period = 1/t_{SK} (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the statement. Within the SK period, both t_{OH} and t_{CS} limits must be observed. Therefore, it is not advisable to set 1/t_{SK} = 1/(t_{OH} + t_{CS}) + t_{CS} + t_{OH}.

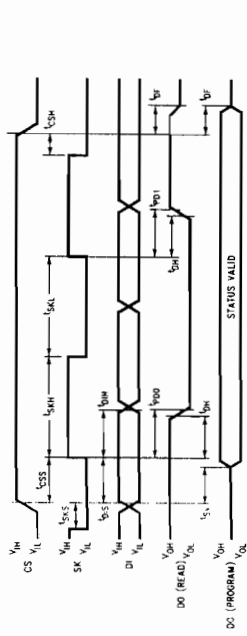
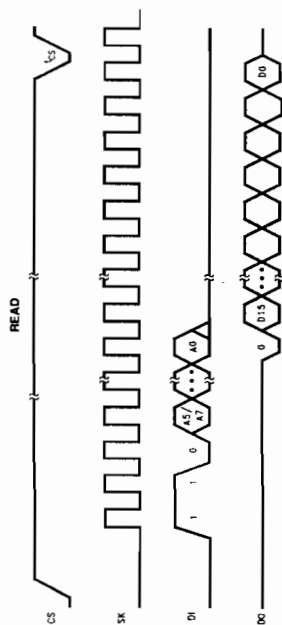
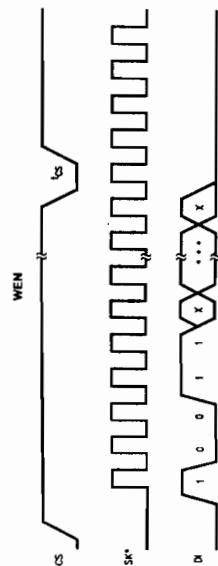
AC Test Conditions

V _{CC} Range	V _L /V _H Input Levels	V _L /V _H Timing Level	V _{CC} /V _{OH} Timing Level	I _{OL} /I _{OH}
4.5V < V _{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	-2.1 mA/0.4 mA

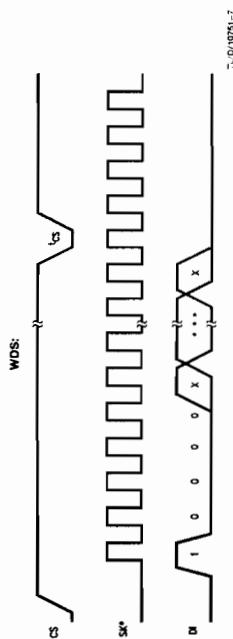
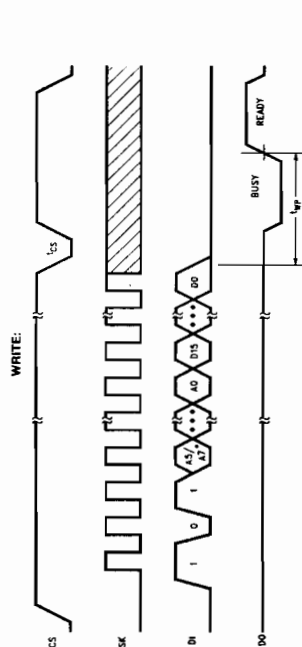
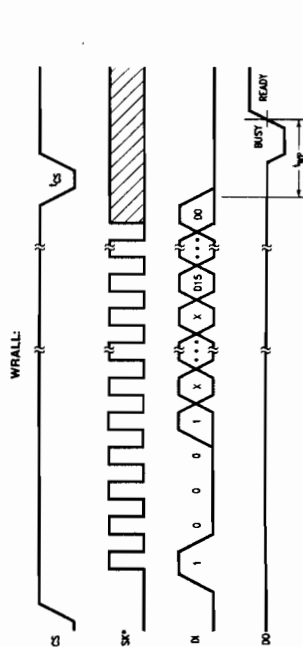
Output Load: 1 TTL Gate (C_L = 100 pF)

Timing Diagrams

Synchronous Data Timing

T_{UD}/10751-4T_{UD}/10751-3T_{UD}/10751-6

Timing Diagrams (Continued)

T_{UD}/10751-7T_{UD}/10751-8T_{UD}/10751-9



NM93CS06/CS46/CS56/CS66

(MICROWIRE™ Bus Interface) 256-/1024-/2048-/4096-Bit Serial EEPROM with Data Protect and Sequential Read

General Description

The NM93CS06/CS46/CS56/CS66 devices are 256-/1024-/2048-/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. Selected registers can be protected against data modification by programming the Protect Register with the address of the first register to be protected against data modification (all registers greater than, or equal to, the selected address are then protected from further change). Additionally, the address can be "locked" into the device, making all future attempts to change data impossible. These devices are fabricated using National Semiconductor floating-gate CMOS processes for high reliability, high endurance and low power consumption. The NM93CS06/CS46/CS56/CS66 is offered in an SO package for small space considerations.

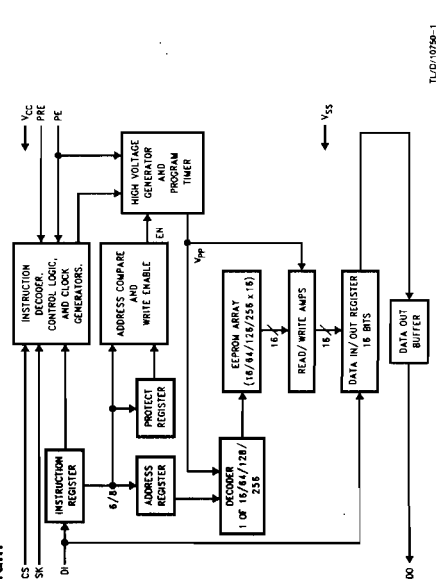
The EEPROM interfacing is MICROWIRE compatible providing instructions for read, write, erase, and protect operations. There are a total of 10 instructions, 5 which operate on the EEPROM memory, and 5 which operate on the Protect Register. The memory instructions are

READ, WRITE, WRITE ALL, WRITE ENABLE, and WRITE DISABLE. The Protect register instructions are PREAD, PWRITE, PRENABLE, PROCLEAR, and PROISABLE.

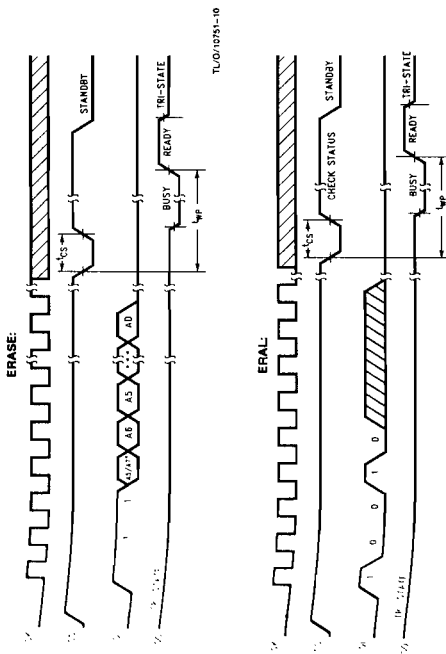
Features

- Write protection in a user defined section of memory
- Sequential register read
- Typical active current of 400 μ A and standby current of 25 μ A
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Soft timed write cycle
- Device status during programming mode
- 40 year data retention
- Endurance: 10^6 data changes
- 4.5V to 5.5V operation in all modes of operation
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



Timing Diagrams (Continued)



TL010751-11